TUL Embedded

E16GMFA-CK

Embedded MXM 3.0 type A Module

CONTENTS

1. Specification

Model Name	E16GMFA-CK
Graphics Engine	AMD Embedded Radeon E9260
Process Node	Fin FET 14 nm
Engine Clock (max)	Up to 1053 MHz
Graphics Memory	128-bit, 4 GB, GDDR5
Memory Clock (max)	1500 MHz / 6.0 Gbps
MXM type	MXM 3.0, Type A
Bus Interface	PCI Express® 3.0 (X8)
Shader Processing Units	896 Shaders
Floating Point Performance	1.9 TFLOPs
DirectX® capability	DirectX® 12
Shader Model	Shader Model 5.0
OpenGL™	OpenGL 4.5
OpenCL™	OpenCL 2.0
VULKAN™	VULKAN™ Support
Unified Video Decoder (UVD)	UVD 6.3 for H.265/HEVC, 4K H.264, VC-1, MPEG-2 MPEG-4 part 2 decode
Power Consumption	50 W
Operating Temperature	0°C ~ 50°C
Dimension	82 x 70 mm

2. Functional Overview

2.1. Memory Interface

AMD Radeon E9260 has four (128-bit) DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel, and must run at the same voltage.

2.2. Acceleration Features

- Support for DirectX® 12 (Feature Level 12_0) features, including the full-speed 32-bit floating point per component operation.
- Shader Model 5.0 geometry and pixel support in a unified shader architecture.
- Support for OpenGL 4.5.
- Support for OpenCL ™ 2.0
- Support for Mantle
- Support for AMD LiquidVR™
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).
- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Angle-invariant algorithm for improved quality.
  - Single- or two-channel data format compatibility.
- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.

- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.3. Display System

The display system supports accelerated display modes on multiple independent display controllers.

The full features of the display system are outlined in the following sections.

- Up to four independent display controllers that support up to true 36-bpp (bits per pixel) throughout the display pipe.
- Support for each display output type up to the following display timings:
  - DisplayPort 1.3 up to two 5120 × 2880 pixel resolution display @ 60 Hz refresh rates on two single stream (SST) DisplayPort 1.3 outputs, and up to four 3840 × 2160 @ 60 Hz or 4096 × 2160 @ 60 Hz displays
  - HDMI™ 2.0a (6 Gbit/s) up to four 3840 × 2160 @ 60 Hz or four 4096 ×2160 @ 60 Hz outputs
  - Dual-link DVI up to two 2560 × 1600 @ 60 Hz or 1920 × 1200 @ 60 Hz
  - Single-link DVI up to four 1920 × 1200 @ 60 Hz
- Support for up to four independent display timings on DisplayPort, HDMI, or DVI interfaces
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling for High Dynamic Range (HDR) or Standard Dynamic Range (SDR)
- HDCP supported independently and simultaneously on all HDMI, DVI, and DisplayPort outputs

  Note: HDCP is available only to licensed HDCP licensees and can only be enabled when connected to an HDCP-capable receiver
  - Supports HDCP version 1.4/2.2 protection for the HDMI interface
  - Supports HDCP version 1.1/2.2 protection for the DisplayPort interface
  - Supports HDCP version 1.4 protection for the DVI interface

- Support for Stereo 3D displays through HDMI, DisplayPort, and DVI. Includes frame-sequential and frame-packed full Stereo 3D modes. Also 2D frame- compatible modes including side-by-side, top-and-bottom, line interleaved, and pixel interleaved
- Line or pixel interleave Stereo 3D mixing supported without the use of graphics shaders by using two display pipes for left and right and blending together immediately before the display output; this improves the Stereo 3D performance.

2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit output when using dual-Link DVI up to 1920 × 1200 @ 60 Hz
- Supports industry-standard CEA-861 video modes including 480p, 720p, 1080i,1080p, and 2160p.
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—594 MP/s

2.5. DisplayPort (DP) Features

- Supports all the mandatory features of the DisplayPort Standard Version 1.3 and the following optional features on all links:
  - HBR3 (8.1 Gbps) support
  - ACM packet-type support
  - ISRC packet-type support
  - Y-only colormetry
- DisplayPort Multi-streaming Transport (MST) allowing up to four display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Each DisplayPort link can support three options for the number of lanes and four options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 8.1-, 5.4-, 2.7-, or 1.62-Gbps link-data rate per lane
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
- The following table shows the maximum pixel rates for four, two, or one lane(s)

at 8.1-Gbps link rate.

	18 bpp	24 bpp	30 bpp	36 bpp
One Lane	360 MP/s	270 MP/s	216 MP/s	180 MP/s
Two Lanes	720 MP/s	540 MP/s	432 MP/s	360 MP/s
Four Lanes	1080 MP/s	1080 MP/s	864 MP/s	720 MP/s

2.6. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, ×8 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×8 lane reversal where the receivers on lanes 0 to 7 on the graphics endpoint are mapped to the transmitters on lanes 7 down to 0 on the root complex.
- Supports ×8 lane reversal where the transmitters on lanes 0 to 7 on the graphics endpoint are mapped to the receivers on lanes 7 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

3. PIN Assignment and Description

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
E1	PWR_SRC_E1	Main power source 7-20V (recommend using 12V) up to 10A.	E2	PWR_SRC_E2	Main power source 7-20V (recommend using 12V) up to 10A.
E3	GND_E3	GND	E4	GND_E4	GND
1	5V_1	5V ±5% 2.5A	2	PRSNT_R#_2	MXM module present detects. Weak pull-up required on system if module detection is desired. Module pin is connected to ground.
3	5V_3	5V ±5% 2.5A	4	WAKE#_4	N/A
5	5V_5	5V ±5% 2.5A	6	PWR_GOOD_6	Power sequencing sideband. The module will assert this signal when all its internal power regulators are within the required tolerance.
7	5V_7	5V ±5% 2.5A	8	PWR_EN_8	Module power enable. System must assert this signal to power on the module. May be asserted only after all input rails are within the specified tolerance.
9	5V_9	5V ±5% 2.5A	10	N/A	N/A
11	GND_11	GND	12	GND_12	GND
13	GND_13	GND	14	RSVD_14	RSVD for HPD.
15	GND_15	GND	16	TESTEN	TESTEN
17	GND_17	GND	18	PWR_LEVEL_18	Signals the module to switch to a lower power state. Modules must reduce the power by at least 20% within 50ms.
19	PEX_STD_SW#	PEX_STD_SW#	20	TH_OVERT#_20	Thermal shutdown request. System must power down the MXM module within 500ms to prevent permanent damage. Pull-up resistor to 3.3V of appropriate value is required on the system board.
21	VGA_DISABLE#	VGA_DISABLE#	22	TH_ALERT#_22	Thermal interrupt request. Signal may be used by the system to signal to module to reduce power consumption. The signal may also be used by the module to signal to the system a non critical temperature alert.

					Pull-up resistor to 3.3V of appropriate value is required on the system board.
23	PNL_PWR_EN_23	Internal panel power enable for LVDS or eDP.	24	TH_PWM_24	Thermal PWM. This signal may be used to control a fan connected to the module thermal solution.
25	PNL_BL_EN_25	Internal panel backlight enable for eDP.	26	GPIO0_26	N/A
27	PNL_PWM_27	Internal panel PWM brightness control.	28	GPIO1_28	N/A
29	HDMI_CEC_29	N/A	30	GPIO2_30	N/A
31	DVI_HPD_31	Used for configuration with five or more display output HPD5.	32	SMB_DAT_32	SMBus Data
33	LVDS_DDC_DAT_33	DP AUX5N (or DVI-D DDC Data).	34	SMB_CLK_34	SMBus Clock
35	LVDS_DDC_CLK_35	DP AUX5P (or DVI-D DDC CLK).	36	GND_36	GND
37	GND_37	GND	38	N/A	N/A
39	OEM_39	N/A	40	N/A	N/A
41	OEM_41	N/A	42	N/A	N/A
43	OEM_43	N/A	44	N/A	N/A
45	OEM_45	N/A	46	GND_46	GND
47	GND_47	GND	48	PEX_TX15#_48	N/A
49	PEX_RX15#_49	N/A	50	PEX_TX15_50	N/A
51	PEX_RX15_51	N/A	52	GND_52	GND
53	GND_53	GND	54	PEX_TX14#_54	N/A
55	PEX_RX14#_55	N/A	56	PEX_TX14_56	N/A
57	PEX_RX14_57	N/A	58	GND_58	GND
59	GND_59	GND	60	PEX_TX13#_60	N/A
61	PEX_RX13#_61	N/A	62	PEX_TX13_62	N/A
63	PEX_RX13_63	N/A	64	GND_64	GND
65	GND_65	GND	66	PEX_TX12#_66	N/A
67	PEX_RX12#_67	N/A	68	PEX_TX12_68	N/A
69	PEX_RX12_69	N/A	70	GND_70	GND
71	GND_71	GND	72	PEX_TX11#_72	N/A
73	PEX_RX11#_73	N/A	74	PEX_TX11_74	N/A
75	PEX_RX11_75	N/A	76	GND_76	GND
77	GND_77	GND	78	PEX_TX10#_78	N/A
79	PEX_RX10#_79	N/A	80	PEX_TX10_80	N/A
81	PEX_RX10_81	N/A	82	GND_82	GND

83	GND_83	GND	84	PEX_TX9#_84	N/A
85	PEX_RX9#_85	N/A	86	PEX_TX9_86	N/A
87	PEX_RX9_87	N/A	88	GND_88	GND
89	GND_89	GND	90	PEX_TX8#_90	N/A
91	PEX_RX8#_91	N/A	92	PEX_TX8_92	N/A
93	PEX_RX8_93	N/A	94	GND_94	GND
95	GND_95	GND	96	PEX_TX7#_96	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
97	PEX_RX7#_97	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	98	PEX_TX7_98	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
99	PEX_RX7_99	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	100	GND_100	GND
101	GND_101	GND	102	PEX_TX6#_102	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
103	PEX_RX6#_103	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	104	PEX_TX6_104	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
105	PEX_RX6_105	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	106	GND_106	GND
107	GND_107	GND	108	PEX_TX5#_108	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
109	PEX_RX5#_109	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	110	PEX_TX5_110	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
111	PEX_RX5_111	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	112	GND_112	GND
113	GND_113	GND	114	PEX_TX4#_114	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)

115	PEX_RX4#_115	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	116	PEX_TX4_116	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
117	PEX_RX4_117	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	118	GND_118	GND
119	GND_119	GND	120	PEX_TX3#_120	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
121	PEX_RX3#_121	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	122	PEX_TX3_122	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
123	PEX_RX3_123	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	124	GND_124	GND
125	GND_125	GND	126	KEY	
127	KEY		128	KEY	
129	KEY		130	KEY	
131	KEY		132	KEY	
133	GND_133	GND	134	GND_134	GND
135	PEX_RX2#_135	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	136	PEX_TX2#_136	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
137	PEX_RX2_137	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	138	PEX_TX2_138	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
139	GND_139	GND	140	GND_140	GND
141	PEX_RX1#_141	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	142	PEX_TX1#_142	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
143	PEX_RX1_143	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	144	PEX_TX1_144	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
145	GND_145	GND	146	GND_146	GND
147	PEX_RX0#_147	PCI Express input to the Root Complex.	148	PEX_TX0#_148	PCI Express output from the Root Complex.

		DC blocking caps must be placed on the system board.			DC blocking caps must be placed on the system board. (-)
149	PEX_RX0_149	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	150	PEX_TX0_150	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
151	GND_151	GND	152	GND_152	GND
153	PEX_REFCLK#_153	PCI Reference Clock Differential Clock (-)	154	CLK_REQ#_154	PCI Express clock request. Pull-up resistor to 3.3V is required on the system board if the function is supported
155	PEX_REFCLK_155	PCI Reference Clock Differential Cock (+)	156	PEX_RST#_156	PCI Express reset signal.
157	GND_157	GND	158	VGA_DDC_DAT_158	VGA DDC Data.
159	JTAG_TDO_159	JTAG_TDO	160	VGA_DDC_CLK_160	VGA DDC Clock.
161	JTAG_TDI_161	JTAG_TDI	162	VGA_VSYC_162	N/A
163	JTAG_TCLK_163	JTAG_TCLK	164	VGA_HSYC_164	N/A
165	JTAG_TMS_165	JTAG_TMS	166	GND_166	GND
167	JTAG_TRSTB_167	JTAG_TRSTB	168	VGA_RED_168	N/A
169	LVDS_UCLK#_169	N/A	170	VGA_GREEN_170	N/A
171	LVDS_UCLK_171	N/A	172	VGA_BLUE_172	N/A
173	GND_173	GND	174	GND_174	GND
175	LVDS_UTX3#_175	N/A	176	LVDS_LCLK#_176	DPE_3N (single- link DVI-D TMDS CLKN). DC blocking caps for DPE must be placed on the system board.
177	LVDS_UTX3_177	N/A	178	LVDS_LCLK_178	DPE_3P (single- link DVI-D TMDS CLKP). DC blocking caps for DPE must be placed on the system board.
179	GND_179	GND	180	GND_180	GND
181	LVDS_UTX2#_181	N/A	182	LVDS_LTX3#_182	N/A
183	LVDS_UTX2_183	N/A	184	LVDS_LTX3_184	N/A
185	GND_185	GND	186	GND_186	GND
187	LVDS_UTX1#_187	N/A	188	LVDS_LTX2#_188	DPE_0N (single-link DVI-D TMDS DATA_2N). DC blocking caps for DPE must be placed on the system board.
189	LVDS_UTX1_189	N/A	190	LVDS_LTX2_190	DPE_0P (single-link DVI-D TMDS DATA_2P). DC blocking caps for DPE must be placed on the system board.

191	GND_191	GND	192	GND_192	GND
193	LVDS_UTX0#_193	N/A	194	LVDS_LTX1#_194	DPE_1N (single-link DVI-D TMDS DATA_1N). DC blocking caps for DPE must be placed on the system board.
195	LVDS_UTX0_195	N/A	196	LVDS_LTX1_196	DPE_1P (single-link DVI-D TMDS DATA_1P). DC blocking caps for DPE must be placed on the system board.
197	GND_197	GND	198	GND_198	GND
199	DP_C_L0#_199	DPC_0N (dual-link DVI-D TMDS Data_5N, or single-link DVI-D TMDS Data_2N, or HDMI™ TMDS Data_2N). DC blocking caps for DPC must be placed on the system board.	200	LVDS_LTX0#_200	DPE_2N (single-link DVI-D TMDS DATA_0N). DC blocking caps for DPE must be placed on the system board.
201	DP_C_L0_201	DPC_0P (dual-link DVI-D TMDS Data_5P, or single-link DVI-D TMDS Data_2P, or HDMI TMDS Data_2P). DC blocking caps for DPC must be placed on the system board.	202	LVDS_LTX0_202	DPE_2P (single-link DVI-D TMDS DATA_0P). DC blocking caps for DPE must be placed on the system board.
203	GND_203	GND	204	GND_204	GND
205	DP_C_L1#_205	DPC_1N (dual-link DVI-D TMDS Data_4N, or single-link DVI-D TMDS Data_1N, or HDMI TMDS Data_1N). DC blocking caps for DPC must be placed on the system board.	206	DP_D_L0#_206	DPD_0N (dual-link DVI-D TMDS Data_5N, or single-link DVI-D TMDS Data_2N, or HDMI TMDS Data_2N). DC blocking caps for DPD must be placed on the system board.
207	DP_C_L1_207	DPC_1P (dual-link DVI-D TMDS Data_4P, or single-link DVI-D TMDS Data_1P, or HDMI TMDS Data_1P). DC blocking caps for DPC must be placed on the system board.	208	DP_D_L0_208	DPD_0P (dual-link DVI-D TMDS Data_5P, or single-link DVI-D TMDS Data_2P, or HDMI TMDS Data_2P). DC blocking caps for DPD must be placed on the system board.
209	GND_209	GND	210	GND_210	GND
211	DP_C_L2#_211	DPC_2N (or dual-link DVI-D TMDS Data_3N, or single-link DVI-D TMDS Data_0N, or HDMI TMDS Data_0N). DC blocking caps for DPC must be placed on the system board.	212	DP_D_L1#_212	DPD_1N (dual-link DVI-D TMDS Data_4N, or single-link DVI-D TMDS Data_1N, or HDMI TMDS Data_2N). DC blocking caps for DPD must be placed on the system board.
213	DP_C_L2_213	DPC_2P (dual-link DVI-D TMDS Data_3P, or single-link DVI-D TMDS	214	DP_D_L1_214	DPD_1P (dual-link DVI-D TMDS Data_4P, or single-link DVI-D TMDS Data_1P, or HDMI™

		Data_0P, or HDMI TMDS Data_0P). DC blocking caps for DPC must be placed on the system board.			TMDS Data_1P). DC blocking caps for DPD must be placed on the system board.
215	GND_215	GND	216	GND_216	GND
217	DP_C_L3#_217	DPC_3N (single-link DVI-D TMDS CLK_N, or HDMI™ TMDS CLK_N. No connection for dual-link DVI-D). DC blocking caps for DPC must be placed on the system board.	218	DP_D_L2#_218	DPD_2N (dual-link DVI-D TMDS Data_3N, or single-link DVI-D TMDS Data_0N, or HDMI TMDS Data_0N). DC blocking caps for DPD must be placed on the system board.
219	DP_C_L3_219	DPC_3P (single-link DVI-D TMDS CLK_P, or HDMI TMDS CLK_P. No connection for dual-link DVI-D). DC blocking caps for DPB must be placed on the system board.	220	DP_D_L2_220	DPD_2P (dual-link DVI-D TMDS Data_3P, or single-link DVI-D TMDS Data_0P, or HDMI TMDS Data_0P). DC blocking caps for DPD must be placed on the system board.
221	GND_221	GND	222	GND_222	GND
223	DP_C_AUX#_223	DPC AUX3N (or DDC Data for DVI-D or HDMI).	224	DP_D_L3#_224	DPD_3N (single-link DVI-D TMDS CLK_N, or HDMI TMDS CLK_N. No connection for dual-link DVI-D). DC blocking caps for DPD must be placed on the system board.
225	DP_C_AUX_225	DPC AUX3P (or DDC Clock for DVI-D or HDMI).	226	DP_D_L3_226	DPD_3P (single-link DVI-D TMDS CLK_P, or HDMI TMDS CLK_P. No connection for dual-link DVI-D). DC blocking caps for DPD must be placed on the system board.
227	RSVD_227	N/A	228	GND_228	GND
229	RSVD_229	N/A	230	DP_D_AUX#_230	DPD AUX4N (or DDC Data for DVI-D or HDMI)
231	RSVD_231	N/A	232	DP_D_AUX_232	DPD AUX4P (or DDC Clock for DVI-D or HDMI)
233	RSVD_233	N/A	234	DP_C_HPD_234	Hotplug detect. Protection circuit must be placed on the system board. (HPD3)
235	RSVD_235	N/A	236	DP_D_HPD_236	Hotplug detect. Protection circuit must be placed on the system board. (HPD4)
237	RSVD_237	N/A	238	N/A	N/A
239	RSVD_239	N/A	240	3V3_240	3.3V ±5% 1A
241	RSVD_241	N/A	242	3V3_242	3.3V ±5% 1A
243	RSVD_243	N/A	244	GND_244	GND

245	RSVD_245	N/A	246	DP_B_L0#_246	DP B _0N (dual-link DVI-D TMDS Data_2N, or single-link DVI-D TMDS Data_2N, or HDMI TMDS Data_2N). DC blocking caps for DPB must be placed on the system board.
247	RSVD_247	N/A	248	DP_B_L0_248	DP B _0P (dual-link DVI-D TMDS Data_2P, or single-link DVI-D TMDS Data_2P, or HDMI TMDS Data_2P). DC blocking caps for DPB must be placed on the system board.
249	RSVD_249	N/A	250	GND_250	GND
251	GND_251	GND	252	DP_B_L1#_252	DPB_1N (dual-link DVI-D TMDS Data_1N, or single-link DVI-D TMDS Data_1N, or HDMI™ TMDS Data_1N). DC blocking caps for DPB must be placed on the system board.
253	DP_A_L0#_253	DPA_0N (dual-link DVI-D TMDS Data_2N, or single-link DVI-D TMDS Data_2N, or HDMI TMDS Data_2N). DC blocking caps for DPA must be placed on the system board.	254	DP_B_L1_254	DPB_1P (dual-link DVI-D TMDS Data_1P, or single-link DVI-D TMDS Data_1P, or HDMI TMDS Data_1P). DC blocking caps for DPB must be placed on the system board.
255	DP_A_L0_255	DPA_0P (dual-link DVI-D TMDS Data_2P, or single-link DVI-D TMDS Data_2P, or HDMI TMDS Data_2P). DC blocking caps for DPA must be placed on the system board.	256	GND_256	GND
257	GND_257	GND	258	DP_B_L2#_258	DPB_2N (dual-link DVI-D TMDS Data_0N, or single-link DVI-D TMDS Data_0N, or HDMI TMDS Data_0N). DC blocking caps for DPB must be placed on the system board.
259	DP_A_L1#_259	DPA_1N (dual-link DVI-D TMDS Data_1N, or single-link DVI-D TMDS Data_1N, or HDMI TMDS Data_1N). DC blocking caps for DPA must be placed on the system board.	260	DP_B_L2_260	DPB_2P (dual-link DVI-D TMDS Data_0P, or single-link DVI-D TMDS Data_0P, or HDMI TMDS Data_0P). DC blocking caps for DPB must be placed on the system board.
261	DP_A_L1_261	DPA_1P (dual-link DVI-D TMDS Data_1P, or single-link DVI-D TMDS Data_1P, or HDMI TMDS Data_1P). DC blocking caps for DPA must be placed on the system board.	262	GND_262	GND

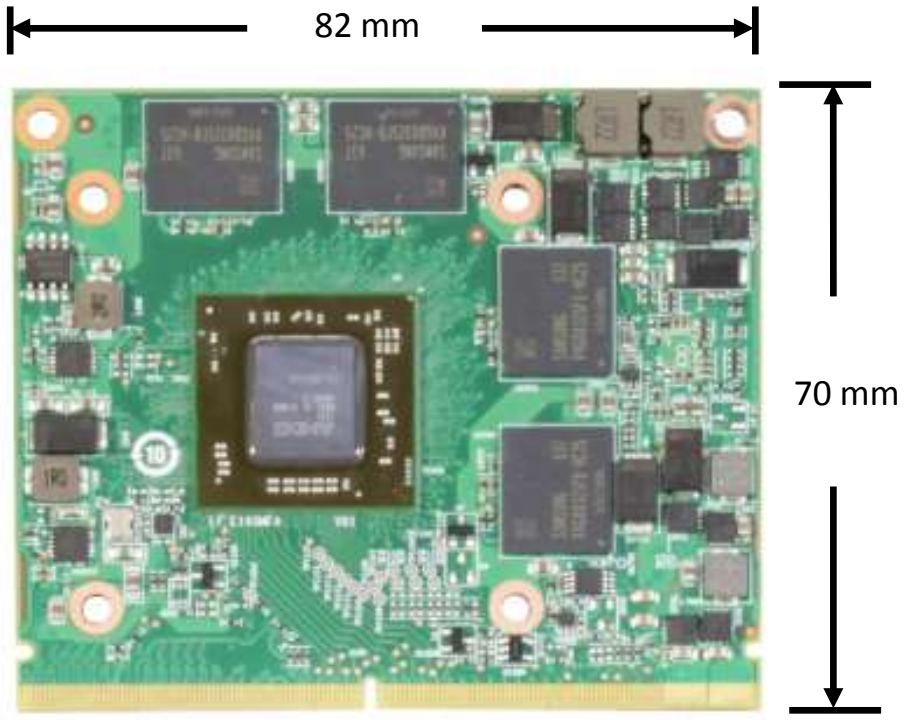
263	GND_263	GND	264	DP_B_L3#_264	DPB_3N (dual-link DVI-D TMDS CLK_N, or single-link DVI-D TMDS CLK_N, or HDMI TMDS CLK_N). DC blocking caps for DPB must be placed on the system board.
265	DP_A_L2#_265	DPA_2N (dual-link DVI-D TMDS Data_0N, or single-link DVI-D TMDS Data_0N, or HDMI TMDS Data_0N). DC blocking caps must be placed on the system board	266	DP_B_L3_266	DPB_3P (dual-link DVI-D TMDS CLK_P, or single-link DVI-D TMDS CLK_P, or HDMI TMDS CLK_P). DC blocking caps for DPB must be placed on the system board.
267	DP_A_L2_267	DPA_2P (dual-link DVI-D TMDS Data_0P, or single-link DVI-D TMDS Data_0P, or HDMI TMDS Data_0P). DC blocking caps for DPA must be placed on the system board.	268	GND_268	GND
269	GND_269	GND	270	DP_B_AUX#_270	DPB AUX2N (or DDC Data for DVI-D or HDMI).
271	DP_A_L3#_271	DPA_3N (dual-link DVI-D TMDS CLK_N, or single-link DVI-D TMDS CLK_N, or HDMI TMDS CLK_N). DC blocking caps for DPA must be placed on the system board.	272	DP_B_AUX_272	DPB AUX2P (or DDC Clock for DVI-D or HDMI)
273	DP_A_L3_273	DPA_3P (dual-link DVI-D TMDS CLK_P, or single-link DVI-D TMDS CLK_P, or HDMI TMDS CLK_P). DC blocking caps for DPA must be placed on the system board.	274	DP_B_HPD_274	Hotplug Detection. Protection circuit must be placed on the system board (HPD2)
275	GND_275	GND	276	DP_A_HPD_276	Hotplug detect. Protection circuit must be placed on the system board (HPD1).
277	DP_A_AUX#_277	DPA AUX1N (or DDC Data for DVI-D or HDMI).	278	3V3_278	3.3V ±5% 1A
279	DP_A_AUX_279	DPA AUX1P (or DDC Clock for DVI-D or HDMI).	280	3V3_280	3.3V ±5% 1A
281	PRSNT_L#_281	MXM module present detects. Weak pull-up required on system if module detection is desired. Module pin is connected to ground.			

Note : E9260 comes with 5 TMDS, PCI-E X8, and no CRT output.

4. Board Configuration

4.1 Board Dimension

(Unit : mm)



Change log list

Rev.	Data	History
1.0	2017/03/01	E16GMFA-CK datasheet